Differences between the MT8972A and the MT8972B

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This application sheet compares the new MT8972B functionality with that of the MT8972A. All changes to the MT8972B have been designed so that backward compatibility with the MT8972A is maintained.

L_{OUT} Dis

This pin is labelled NC on the MT8972A and carries no functionality. Users are requested to leave it open circuited.

The MT8972B user is given the ability to control the device's transmit signal energy on L_{OUT}. This function is useful in applications where specifications may stipulate that no transmit energy is allowed until the line type has been verified.

Pulling this pin (L_{OUT} DIS) low allows the device transmitter to function normally, as in the MT8972A. Pulling this pin high will disable the transmitter (idles at VBias). This pin, in the MT8972B, has an internal pull-down resistor so that it may be used in designs for, and operate the same as, the MT8972A.

Precanceller Bypass

This pin has no function in the MT8972A and users are requested to leave it open circuited.

The MT8972B user may bypass the internal precanceller thus isolating the transmit and receive signal paths completely. This allows precancellation to be designed into external functions, such as loop extenders, under the control of the designer.

Pulling this pin (Procaine) low allows the internal precanceller to function normally, as in the MT8972A. Pulling this pin high will disable the internal precanceller. This pin in the MT8972B has an internal pull-down resistor so that it may be used in designs for, and operate the same as, the MT8972A.

Diagnostics Register Reset

Bit 2 of the MT8972A control register is not used and the user is asked to write this bit logic low.

The MT8972B user may use this bit to control how the diagnostics register is reset.

Writing this bit (DRR) low will cause the diagnostics register to be reset coincident with the next frame

ITEM	MT8972A	MT8972B
L_{OUT} DIS	Pin 19. Leave as no connect. Pin number refers to DIP packaging	Pin19. Transmit line output disable.
Precanceller Bypass (Precan)	Pin 18. Leave as no connect. Pin number refers to DIP packaging.	Pin 18. Precanceller bypass option.
Diagnostics Reset	Bit 2 of Control Register. Not used.	Bit 2 of Control Register. Diagnostics Register reset control.
ID Bit	Bit 7 of Status Register. Will return a “1” when read.	Bit 7 of Status Register. Will return a “0” when read.
Temperature	0°C to +70°C.	-40°C to +85°C.
Housekeeping Bit	Single buffered to/from line.	Double buffered to/from line.
Relative Clock Phase (MAS/DN Mode)	t_{W1}: restricted window starts 17ns before $\overline{C4}$ falling edge. t_{W2}: restricted window extends 24ns after $\overline{C4}$ falling edge.	No restricted window.
L_{OUT} Amplitude	Maximum L_{OUT} peak-to-peak voltage is slightly reduced (by 0.2V p-p) in the MT8972B to avoid clipping of the output waveform.	

Table 1. Item Summary

pulse as occurs in the MT8972A. Writing this bit high will cause the diagnostics register to not be reset. This allows the use of diagnostic functions without the need to continually access the diagnostics register.

ID Bit

Bit 7 of the MT8972A status register will return logic “1” when read. The same bit (ID) in the MT8972B will return logic “0“ when read. This acts as a software identification of the part.

Temperature

The MT8972A is specified for the 0°C to + 70°C range. The MT8972B temperature range has been extended and is specified from -40°C to +85°C.

Housekeeping Bit

The MT8972B housekeeping bit, on the C-channel, is double buffered so that it maintains the same relative timing through the device as the 2B+D channels. The MT8972A employs single buffering of the housekeeping bit.

Relative Clock Phase

There is an input clock timing consideration when the MT8972A is operating in MAS/DN Mode. The OSC2 (10.24 MHz) clock rising edge must not occur within a timing window beginning 17ns before, and extending to 24ns after, the C4 clock falling edge.

This timing window includes the maximum allowable jitter specification of 15ns This implies that when clocks, with guaranteed jitter of less than 15ns are used, the timing window may be reduced accordingly.

There are no clock phase restrictions when using the MT8972B device.

L_{OUT} Amplitude

The maximum Lout peak-to-peak signal voltage is reduced approximately 0.2vp-p in the MT8972B to avoid clipping of the output waveform. This does not affect specified loop length performance.